

## CLAIMS

What is claimed is:

- 1 1. A method, comprising:  
2 reading a status of a buffer used to receive network packets transmitted from a  
3 different chip; and  
4 transmitting to said different chip an unscheduled flow control packet including  
5 information about the status of the buffer.
- 1 2. The method of claim 1, wherein the buffer is associated with a port through  
2 which the network packets travel.
- 1 3. The method of claim 1, wherein the buffer is associated with an aggregate of  
2 ports through which different ones of the network packets travel.
- 1 4. The method of claim 1, wherein the network packets are Internet protocol ("IP")  
2 packets.
- 1 5. The method of claim 1, wherein each network packet is associated with a port  
2 through which the network packet will travel.
- 1 6. A method, comprising:  
2 receiving a network packet from a sender chip, wherein the network packet was  
3 transmitted during a first period;  
4 storing the network packet in a packet buffer, wherein the packet buffer is  
5 associated with a port through which the network packet will travel;  
6 generating an unscheduled flow control packet, wherein the unscheduled flow  
7 control packet comprises information relating to the packet buffer; and

8 transmitting the unscheduled flow control packet to the sender chip, wherein the  
 9 unscheduled flow control packet is transmitted during a second period, and wherein the  
 10 second period is shorter than the first period.

1 7. The method of claim 6, wherein the unscheduled flow control packet comprises  
 2 control data and port data.

1 8. The method of claim 7, wherein the port data comprises a bit pattern that is  
 2 associated with the packet buffer being used in the aggregate.

1 9. The method of claim 7, wherein the control data requires one clock cycle for  
 2 transmission during the second period, and wherein the port data requires four clock  
 3 cycles for transmission during the second period.

1 10. The method of claim 7, wherein the control data includes a command from the  
 2 Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

1 11. A method comprising:  
 2 periodically receiving network packets from a sender chip;  
 3 storing the network packets in a packet buffer; and  
 4 periodically transmitting flow control data back to the sender chip based on a  
 5 status of the packet buffer and without regard to a calendar, wherein the flow control  
 6 data comprises information relating to the packet buffer, and wherein each of said  
 7 periodic transmissions of flow control data is faster than transmission of one of said  
 8 network packets.

1 12. The method of claim 11, wherein the packet buffer is associated with a port  
 2 through which the network packets travel.

1 13. The method of claim 11, wherein the packet buffer is associated with an  
2 aggregate of ports through which different ones of the network packets travel.

1 14. The method of claim 11, wherein the network packets are Internet protocol  
2 ("IP") packets.

1 15. The method of claim 11, wherein each network packet is associated with a port  
2 through which the network packet will travel.

1 16. A method, comprising:  
2 receiving an unscheduled flow control packet from a different chip; and  
3 modifying a rate at which a network packet is transmitted to said different chip,  
4 based on information in the unscheduled flow control packet.

1 17. The method of claim 16, wherein the recipient unit includes a buffer, wherein  
2 the unscheduled flow control packet comprises control data and port data, and wherein  
3 the unscheduled flow control packet is associated with the buffer.

1 18. The method of claim 17, wherein the buffer is associated with an aggregate of  
2 ports through which different ones of the network packets travel, and wherein the port  
3 data comprises a bit pattern that that is associated with the buffer being used in the  
4 aggregate among all available ports.

1 19. The method of claim 17, wherein the buffer is associated with a port through  
2 which the network packet will travel, and wherein the port data comprises a bit pattern  
3 that corresponds to the address of the port.

1 20. The method of claim 17, wherein the control data includes a command from the  
2 Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

1 21. A method, comprising:  
2 receiving an unscheduled flow control packet from a recipient chip during a  
3 second period, wherein the second period is shorter than a first period during which a  
4 network packet is transmitted to the recipient chip, wherein the unscheduled flow  
5 control packet comprises information relating to a packet buffer within the recipient  
6 chip, and wherein the packet buffer is associated with a port; and  
7 modifying a rate at which network packets are transmitted to the recipient chip  
8 based on the information in the unscheduled flow control packet.

1 22. The method of claim 21, wherein the unscheduled flow control packet  
2 comprises control data and port data.

1 23. The method of claim 22, wherein the port data comprises a bit pattern that that  
2 is associated with the packet buffer being used in the aggregate among all available  
3 ports.

1 24. The method of claim 23, wherein the port data comprises a bit pattern that  
2 corresponds to the address of the port.

1 25. The method of claim 23, wherein the control data requires one clock cycle for  
2 transmission during the second period, and wherein the port data requires four clock  
3 cycles for transmission during the second period.

1 26. The method of claim 23, wherein the control data includes a command from the  
2 Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

1 27. A chip, comprising:  
2 a packet buffer to store network packets transmitted from a different chip,  
3 wherein the packet buffer is associated with one or more of a plurality of ports through  
4 which the network packets travel; and  
5 control circuitry, coupled with a packet data bus to receive said network packets  
6 from the different chip, and coupled with an unscheduled flow control packet bus to  
7 generate and transmit unscheduled flow control packets to the different chip, wherein  
8 the unscheduled flow control packets contain information relating to the packet buffer.

1 28. The chip of claim 27, wherein the unscheduled flow control packet comprises  
2 control data and port data.

1 29. The chip of claim 28, wherein the packet buffer is associated with all of the  
2 plurality of ports, and wherein the port data comprises a bit pattern that is associated  
3 with the packet buffer being used in the aggregate among all available ports.

1 30. The chip of claim 29, wherein the packet buffer is associated with one of the  
2 plurality of ports , and wherein the port data comprises a bit pattern that corresponds to  
3 the address of the port.

1 31. A chip, comprising:  
2 flow control logic, coupled with an unscheduled flow control packet bus to  
3 receive an unscheduled flow control packet from a different chip; and  
4 network packet logic, coupled with a packet data bus and the flow control logic,  
5 to modify, in response to the unscheduled flow control packet, a rate at which network  
6 packets are transmitted to the different chip, wherein each of the network packets is  
7 associated with one of a plurality of ports through which that network packet will  
8 travel.

1 32. The chip of claim 31, wherein the different chip includes a buffer, wherein the  
2 unscheduled flow control packet comprises control data and port data, and wherein the  
3 unscheduled flow control packet is associated with the buffer.

1 33. The chip of claim 32, wherein the buffer is associated with all of the plurality of  
2 ports, and wherein the port data comprises a bit pattern that that is associated with the  
3 buffer being used in the aggregate among all available ports.

1 34. The chip of claim 32, wherein the buffer is associated with one of the plurality  
2 of ports through which the network packet will travel, and wherein the port data  
3 comprises a bit pattern that corresponds to the address of the port.

1 35. The chip of claim 32, wherein the control data includes a command from the  
2 Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.